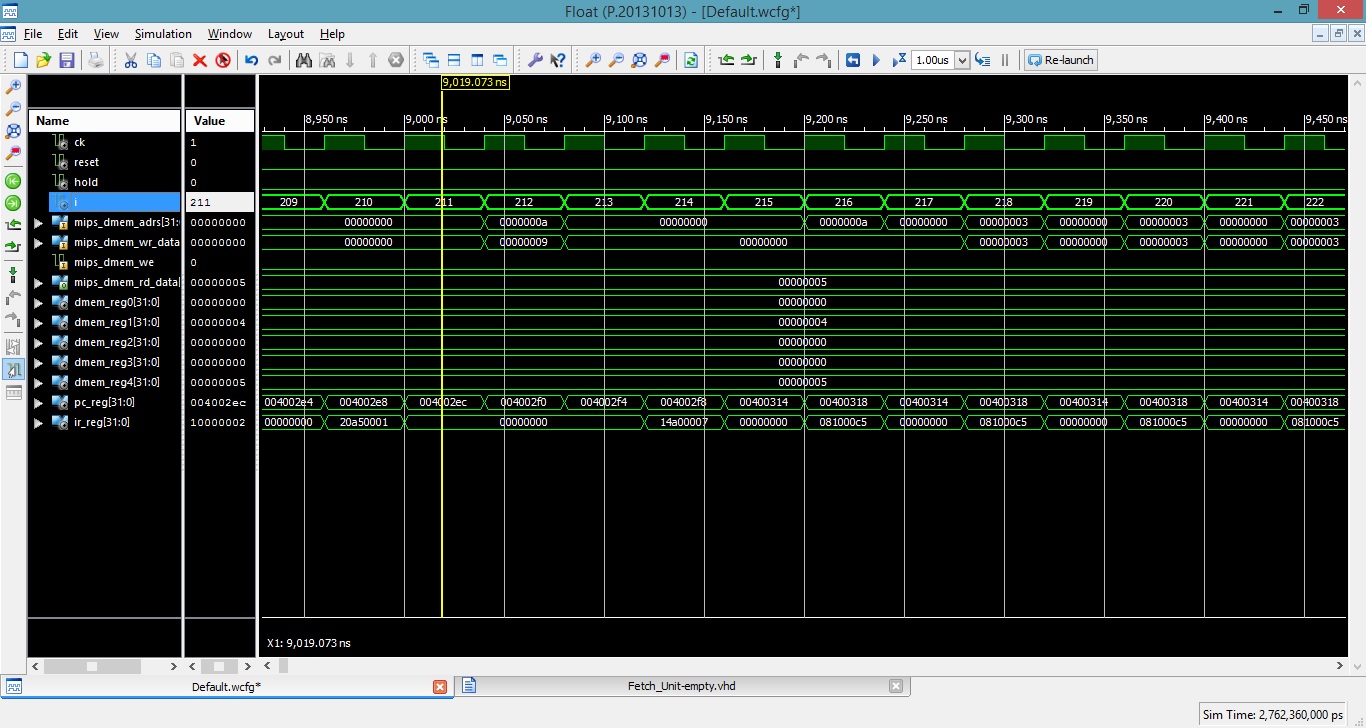
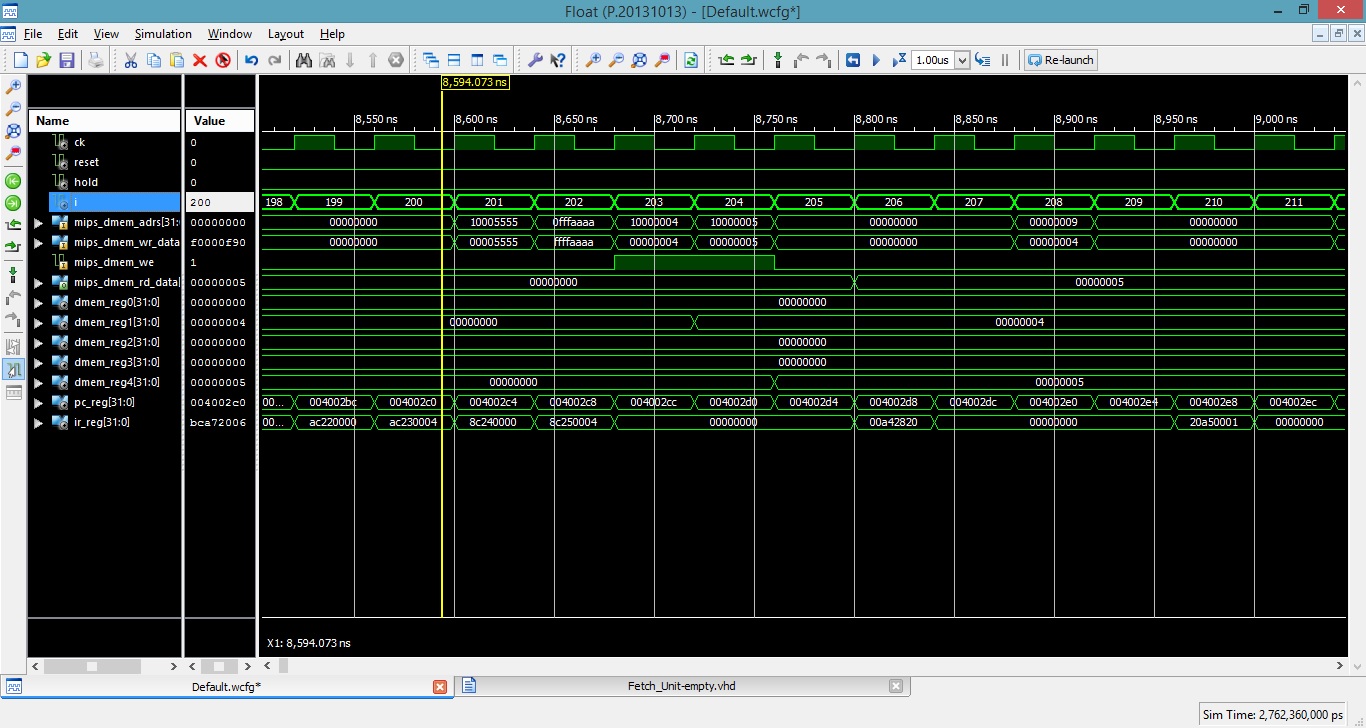
HW5 Report

3.1

200-210:  
  
 210-220:



3.2 We can see that the Assembly program is running: we see 2 writes and 2 reads from the the memory, then we have 3 NOPS between every 2 instruction. Then we enter a loop (jump/branch)

3.3 There should be 3 NOPs between two R-TYPE instructions.

3.4 The limitation is that the register being tested is also used for calculation in the same time, and might be changed, and the BEQ won't notice the change.

3.5 a) While jump operations are executed, the next operations are being fetched & decoded. Can be prevented by NOPs or forwarding.

b) The limitation in 3.4 can be solved by NOPs and Data Forwarding.

c) sw & lw can face MEM hazards, solved by forwarding.